LOW TEMPERATURE SILICON WAFER BONDING FOR MEMS APPLICATIONS

A. A. Ayón[1], X. Zhang[2], K. Turner[3], D. Choi[3], B. Miller[3], S. Nagle[3] and S. M. Spearing[3]
[1]Sony Semiconductor, 1 Sony Place, San Antonio, TX 78245, USA
[2]Department of Manufacturing Engineering, Boston University, Boston, MA 02215, USA
[3]Gas Turbine Laboratory, Massachusetts Institute of Technology, Cambridge, MA 02139, USA

ABSTRACT

This paper reports the investigation of low-temperature silicon wafer fusion bonding for MEMS applications. A bonding process utilizing annealing temperatures between 400ºC and 1100ºC was characterized. The silicon-silicon bonded interface was analyzed by Infrared Transmission (IT) and Transmission Electron Microscopy (TEM) and the bond strength was quantified by a four-point bending-delamination technique.

INTRODUCTION

Silicon wafer-level fusion bonding has been identified as an enabling technology [1, 2] applicable in a large variety of MEMS projects and structures [3], for preparing silicon-on-insulator substrates [4] and for demonstrating packaging schemes at the wafer level. Silicon fusion bonding is an attractive approach for fabricating intricate MEMS structures because it eliminates thermal mismatch problems and has the potential to achieve bonds with strengths comparable to that of bulk silicon. This technique is currently being successfully applied in the emerging field of Power MEMS that typically involves complex structures made possible through the dry-etching and bonding of several silicon wafers. For example, the MIT micro-engine project relies on creating reliable structures involving 6 or more silicon wafers that are fusion-bonded [5]. The technique has also been applied for demonstrating at the micro scale combustors [6], heat exchangers [7] and rocket engines [8] among other applications. There is, therefore, an ever-increasing need for understanding and tailoring the processes taking place during wafer bonding to achieve the objectives of microprocessing compatibility and device reliability. Annealing steps performed at low temperatures to avoid jeopardizing the electrical behavior of active devices or the integrity of thin metallic films are of particular interest in the field. For this purpose we have explored the bonding process for annealing temperatures from 500*ºC* to 1100*ºC* varying surface preparation conditions, residual gas ambient and pressure during wafer contacting, as well as annealing times.

EXPERIMENTAL PROCEDURES

The work was performed with 4", <100> prime, unpatterned silicon wafers of resistivity 10-20 *Ω-cm* that underwent an RCA clean prior to contacting. Some pairs were exposed to an additional 1-minute, diluted HF-dip (30:1) immediately after RCA. Subsequent to surface preparation the wafers were contacted either in a N_2 or an O_2 ambient at different chamber pressures utilizing alignment and bonding fixtures from Electronic Visions that have been described elsewhere [9]. The contacting chamber was equipped with a Balzers™ turbopump that permitted to reach pressures of around 0.38 *mT* in less than 20 *minutes*. The contacted pairs were then annealed in a quartz furnace at a fixed temperature while flowing 3 standard liters per minute (SLM) of N_2.

During annealing the bonded pairs were inspected using infrared transmission (IT) [10]. Transmission electron microscopy (TEM) was used for interface inspection and for measuring the crystal misalignment of the bonded wafers. Finally, the bond strength was measured using the four-point bending-delamination technique that has been described elsewhere [11].

EXPERIMENTAL RESULTS

The first phenomenon observed during the annealing cycle was the appearance of voids or bubbles (see Figure 1) detected with IT [12, 13]. The voids become apparent within a few minutes of initiating the annealing step, they subsequently grow with time to reach a maximum diameter of approximately 11.5 *mm*, then the bubbles were observed to recede and finally become undetectable by IT. One of the suggested origins for this phenomenon is the trapping of gases at the wafer interface. Further corroboration of this effect is observed on wafer-pairs contacted at a lower ambient pressure and for which the voids disappeared in a shorter time (see Figure 2). The occurrence of voids also had a strong dependence on annealing temperature and the bubbles were observed to evolve and disappear within shorter periods of time as the annealing temperature was increased (see Figure 3). The times recorded for the bubbles to become undetectable by IT are plotted in Figure 4. For a thermally activated (i.e. Arrhenius) process it is possible to extract the corresponding activation energy of 1.86 *eV*.

The three well-defined circular traces observed in Figures 1 and 2 are thought to originate due to the presence of the mechanical spacers that separate the silicon wafers prior to contacting. In this step and with the spacers still in place the top wafer is bowed by a spring-loaded pin applied at its geometric center which is intended to produce a single bonding front propagating from the center of the wafers towards the periphery at the moment the spacers are retracted. The creation of a single bonding front serves to prevent the entrapment of residual gases within the guarded interface.

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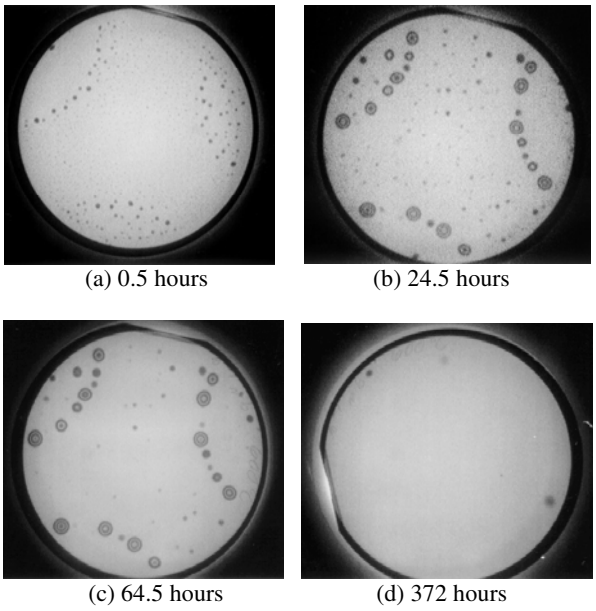
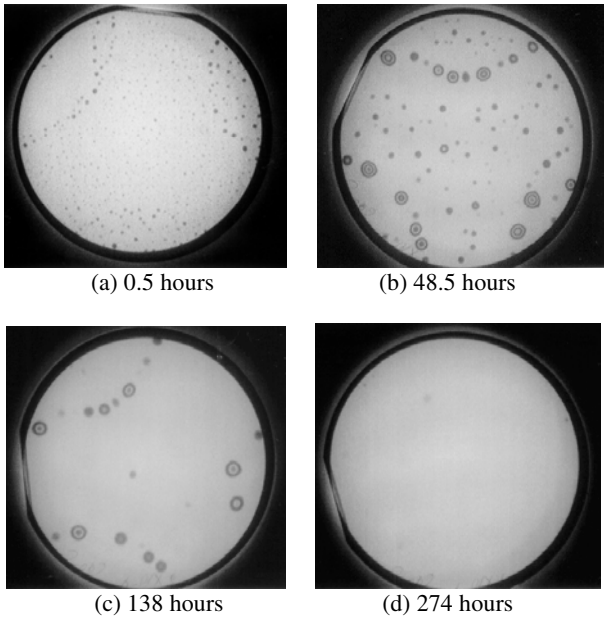


(a) 0.5 hours (b) 24.5 hours

(c) 64.5 hours (d) 372 hours

Figure 1: *Samples contacted in a N_2 ambient, chamber pressure: 75 mT. The samples were then annealed at 600ºC.*



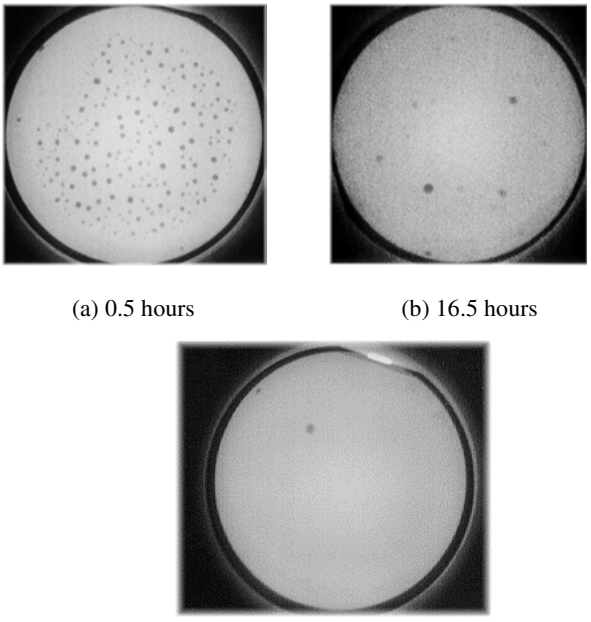
(a) 0.5 hours (b) 48.5 hours

(c) 138 hours (d) 274 hours

Figure 2: *Samples contacted in a N_2 ambient, with a chamber pressure of 0.38 mT and annealed at 600ºC. The voids disappear much sooner compared to samples contacted at higher chamber pressures (see Figure 1).*

Part of the void time evolution characterization involved contacted wafers that had their annealing cycle interrupted and left at atmospheric pressures for periods of time ranging from 2 weeks to 18 months. It was observed that the bubble size and density decreased over time for those samples partially annealed at 600ºC.

However, for the samples that were partially annealed at 400ºC and 500ºC and then left at atmospheric pressure a different behavior pattern emerged. The voids were observed to coalesce over time reaching uncharacteristically large diameters in excess of 15 *mm.* Upon reinitiating the annealing cycle the voids reached diameters in excess of 20 *mm* (see Figure 5) and subsequently the bonded pairs broke in half without delaminating. The same effect was observed on samples contacted in either N_2 or O_2 ambient and for chamber pressures in the range from 0.38 to 75 *mT*.



(a) 0.5 hours (b) 16.5 hours

(c.) 21.5 hours

Figure 3: *Samples contacted in a N_2 ambient, chamber pressure: 38 mT. The samples were subsequently annealed at 700ºC.*

The conditions at the interface between the contacted silicon wafers determine not only the strength of the resulting bond but also whether or not the samples are electrically connected. A variety of projects such as a micro-rocket and many micro-fluidic applications require high bond strengths, and, electrical connection between bonded wafers may be convenient for those applications where the presence of an electric field is required beyond the interface of the bonded pairs. This issue is relevant because complicated through-wafer interconnect schemes can be avoided altogether provided the electrical connection can be tailored. However, the problem posed by the presence of thin layers of silicon dioxide [14, 15] at the interface of the wafers involved can be difficult to overcome. One solution requires the utilization of bonding tools that permit users to perform an *in-situ* silicon dioxide removal immediately prior to bonding, but the bonding equipment in this exercise did not have that capability. Thus, sets of wafers were bonded varying the chemical cleaning procedure before

contacting, namely, by including an additional diluted HF [16] clean after the RCA step but immediately prior to contacting. Other variables explored were chamber pressure and residual gas ambient during contacting. Upon completion of the annealing cycle the interfaces were inspected using TEM.

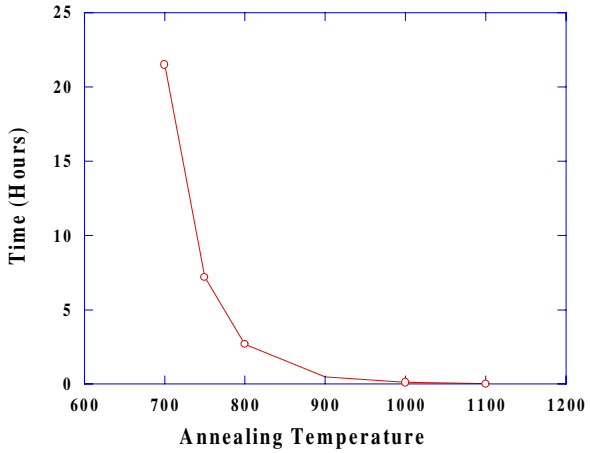


***Figure 4**: Graph showing the observed depenaence of the time needed to clear all voids detected under infrared inspection as a function of annealing temperature (ºC).*

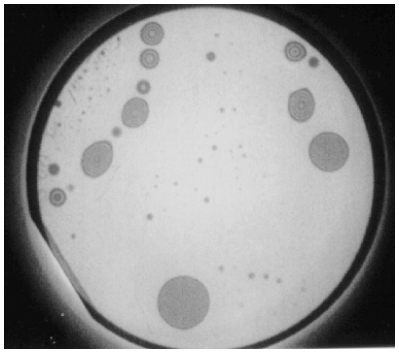
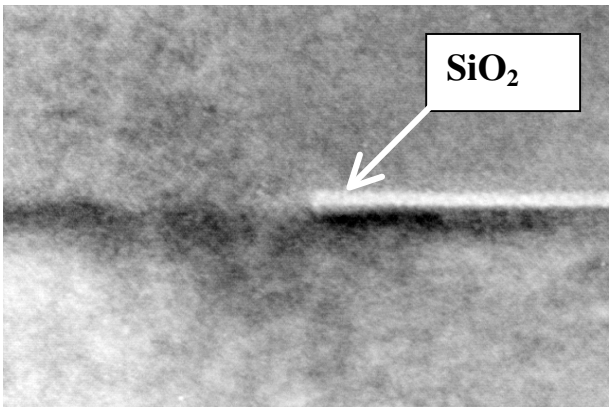
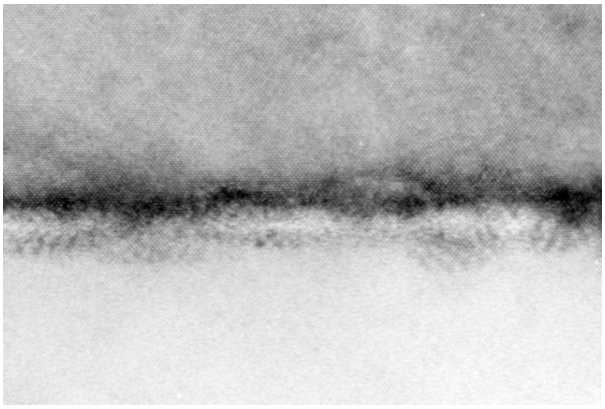


***Figure 5:** Sample annealed for 0.5 hrs at 500ºC and then left at atmosphere for 17 days. The image was collected 30.5 hrs after reinitiating the annealing cycle at 500ºC. Surface migration of trapped nitrogen promotes the emergence of unusually large voids. All samples subsequently broke during annealing.*

The presence of an amorphous silicon dioxide layer at the interface has been linked to the concentration of oxygen interstitials in the bonded wafers and their rotational misorientation [17]. The latter value can be extracted by TEM analysis. It was observed that for rotational misalignments of 2º or less the bonded silicon wafers were electrically connected (see Figure 6) after one hour annealing at 1100ºC and showed no dependence on surface preparation or contacting conditions. Similarly, for rotational misalignments in excess of 2º the presence of the interfacial silicon dioxide layer was observed after the same annealing conditions (see Figure 7).



(a)



(b)

***Figure 6:** TEM inspection of the bonded interfaces of silicon substrates contacted in a residual oxygen ambient at 38 mT. Sample (a) had an additional diluted HF-dip performed prior to contacting and sample (b) solely underwent an RCA clean. The extracted rotational misalignment was 1.5° and 0.6°, respectively.The measured thickness of the discontinuous SiO_2 layer in (a) was 25 Å.*

There are several methods to quantify bond strength, including pressure burst tests, tensile/shear tests and knife–edge tests that are sensitive to the loading configurations and the accuracy when measuring the length of induced cracks. The Maszara method [4], for instance, has a fourth-power dependence on crack length making error propagation a concern when computing bond strengths. Instead, we selected the four-point bending-delamination technique proposed by Charalambides *et al.* [18], thus avoiding the need for measuring crack lengths and its inherent inaccuracy (see Figure 8).

In the Charalambides scheme the strain energy release rate (γ) for crack propagation can be expressed in terms of the moment per unit width (M), the Young's modulus (E), the bottom wafer thickness (h), the thickness ratio of the bottom to the top wafer (ε) and the second moment of area (I). In closed form:

$$\gamma = \frac{M^2}{Eh^3}\left(6\varepsilon^3 - \frac{1}{2I}\right)$$

The results are shown in Figure 9. Maintaining the annealing time fixed at 24 hours, the bond strength increased monotonically but not linearly with increases in the annealing temperature. Furthermore, specimens that were annealed at 900°C and 1000°C were also tested, but failed to delaminate indicating bonds tougher than what can be measured with this method.

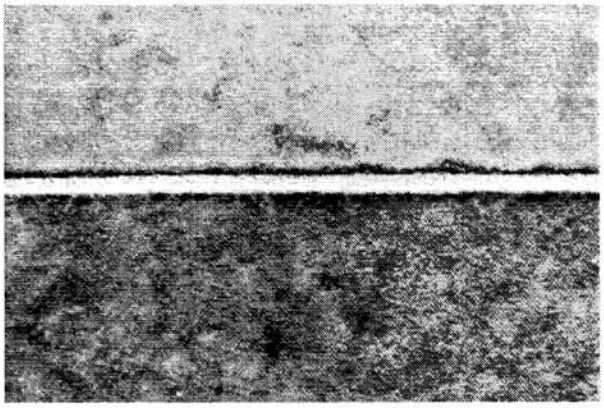


Figure 7: *TEM inspection of the bonded interfaces of silicon substrates contacted in a residual N_2 ambient at 0.38 mT. The sample had an additional diluted HF-dip performed prior to contacting. The extracted rotational misalignment was 3.4°. The measured thickness of the SiO_2 layer was 20 Å. Sample annealed 1 hour at 1100°C.*

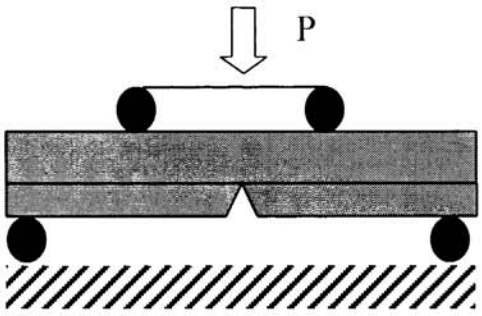


Figure 8: *Schematic of the four-point bend specimen employed in this report.*

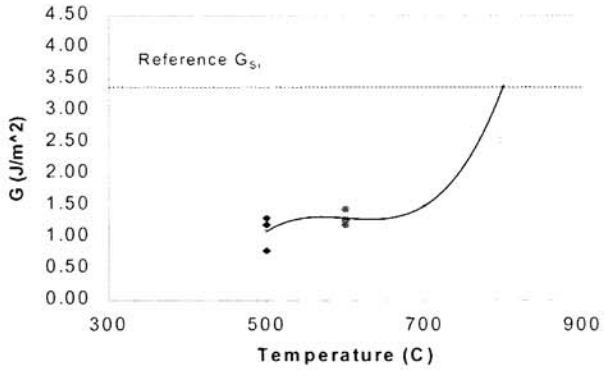


Figure 9: *Bond strength as a function of annealing temperature for a fixed annealing time of 24 hours. Bond strength increases monotonically, but not linearly, with temperature.*

CONCLUSIONS

The paper discusses contacting and annealing procedures to produce bonded wafers which are electrically connected and to achieve targeted bond toughnesses by varying chemical substrate preparation, contacting chamber pressure, residual gas ambient, and annealing temperature and time.

ACKNOWLEDGEMENTS

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